Abstract

An Analysis Method to Predict Performance Requirements for Components of a 4K Resolution Digital TV Platform

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With the recent progress in digital display technology, high-definition digital TVs have emerged, together with new codecs for these TVs. Because these codecs must be highly complex to decode moving pictures with high resolution, a novel multimedia architecture is necessary to implement high-definition digital TVs. This paper suggests a multimedia platform architecture and task mapping for executing a new codec that is under development: namely, a high efficiency video coding (HEVC) decoder. The upper bounds of execution time and memory access of decoder tasks to guarantee quality of service (QoS) were estimated by modeling the main tasks of the HEVC decoder with subtasks and parameter ratios and by analyzing parameter distributions. Performance requirements of the components comprising the multimedia platform architecture were evaluated based on these upper bounds.

Keywords: 4K resolution, Digital TV platform, HEVC, Performance requirements for components

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